CLAIMS:

1. An electronic circuit with an array of programmable logic cells, each of the cells comprising

- an input circuit with a plurality of logic inputs;
- an output circuit;
- a carry input and a carry output, a carry chain coupled between the carry input, the input circuit and the carry output;
- a plurality of programmable logic units, coupled in parallel between the input circuit and the output circuit, the input circuit being configurable between a random logic mode in which each of the programmable logic units receives logic input signals from the same combination of the logic inputs, and a multi-bit operand processing mode in which each of the programmable logic units receives logic input signals from different ones of the logic inputs, the programmable logic units being coupled to successive positions along the carry chain at least in the multi-bit operand mode, so as to process carry signals from the carry chain, the output circuit selecting an output signal from the programmable logic units under control of further input signals in the random logic mode and passing outputs from the programmable logic units in parallel in the multi-bit operand mode.

2. An electronic circuit according to Claim 1, wherein at least one of the programmable logic units comprises

- a configurable look-up table circuit, having an output and inputs coupled to receive the logic input signals from the input circuit;
- a controllable inverter/non-inverter circuit, the output of the look-up table circuit being coupled to the output circuit via the inverter/non-inverter circuit, a carry output of the carry chain being coupled to an inversion non-inversion control input of the inverter/non-inverter circuit.

3. An electronic circuit according to Claim 1, wherein the cell comprises a subtraction control circuit arranged to control at least a carry output determination operation of the carry chain, the carry chain determining a carry output signal from input signals and

carry input signals at each position along the carry chain, control by the subtraction control circuit switching the carry output determination at least between a determination appropriate for addition and determination appropriate for subtraction, under control of a subtraction control signal.

4. An electronic circuit according to Claim 1, wherein the cell comprises a respective multiplication circuit for each programmable logic unit, coupled to multiply at least one of the inputs signals of the programmable logic unit with a multiplicand prior to supplying said at least one of the input signals to an input of the programmable logic unit.

5. An electronic circuit according to Claim 1, wherein each of the programmable logic units has two unit inputs for signals from the logic inputs, each programmable logic unit being configurable to implement independently any two-input bit logic function of the logic inputs.

6. An electronic circuit according to Claim 1, wherein the carry chain circuit has a configurable coupling between said positions and a the carry input of the cell, for configurably supplying either a carry input signal to the carry chain or a standard signal, under control of configuration information from a configuration memory.

7. An electronic circuit according to Claim 1, wherein the carry chain circuit has a plurality of configurable couplings, each coupled between a respective one of said positions and a respective one of the programmable logic units, for configurably supplying either a carry signal from said position to the programmable logic circuit or a further signal that is not a result of propagation through the carry chain, under control of configuration information from a configuration memory.

8. An electronic circuit according to Claim 7, wherein each of the programmable logic units comprises

- a configurable look-up table circuit, having an output and inputs coupled to receive the logic input signals from the input circuit;
- a controllable inverter/non-inverter circuit, the output of the look-up table circuit being coupled to the output circuit via the inverter/non-inverter circuit, the

configurable coupling being coupled to an inversion non-inversion control input of the inverter/non-inverter circuit;

- an exclusive OR circuit, with inputs coupled to inputs of the programmable logic unit and an output configurably coupled to supply the further signal subject to assertion of a multiplex control signal that is common to the programmable logic units.

9. An electronic circuit according to Claim 1, wherein the input circuit is arranged to be configurable to provide only a proper subset of all possible couplings between the signal inputs of the cell and inputs of the programmable logic units, the subset comprising a multi-bit operand coupling, in which respective ones of the signal inputs are coupled to respective inputs of respective ones of the programmable logic units, and a random logic coupling in which a subset of the signal inputs is coupled to the inputs of each of the programmable logic units.

10. An electronic circuit according to Claim 7, wherein the subset comprises a two-bit output random logic coupling in which a first and second subset of the signal inputs are coupled to the inputs of each of a first and second subset of pluralities of the programmable logic units respectively.

11. An electronic circuit according to Claim 1, configured to perform a random logic function, wherein each of the programmable logic units is configured to provide a respective input-output relation and logic input signals from the logic inputs select from which of the programmable logic units a logic output signal is passed to a logic output of the output circuit.

12. An electronic circuit according to Claim 1, configured to perform a multi-bit operand signal processing function, wherein each of the programmable logic units is configured to provide the same input-output relation subject to a carry input signal from the carry chain, and the output circuits outputs output signals from the programmable logic units in parallel.

13. An electronic circuit according to Claim 1, configured to perform a multiplexing function, wherein each of the programmable logic units is configured to pass one of its input signals to an output, and to invert that one of the input signals during said

passing when a multiplexer control signal that is common to the programmable logic units is asserted and the input signals of the programmable logic unit are mutually different.